REMARKS

In the Office Action, Claims 1, 3-6, and 8-27 were examined and are rejected. In response, Claims 1, 4, 6, 8, 9, and 10 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1, 3-6, and 8-27 in view of the following remarks.

I. Objection to the Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. The claimed subject matter in claim 6 is not supported by the specification.

In response, Claim 6 is amended to recite computer readable storage medium (e.g., memory 440 of FIG. 10.) In view of the amendment to Claim 6, please withdraw the objection to the specification.

I. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 1, 3-6, and 8-26 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,275,891 to Dao et al. ("Dao"). Applicants respectfully traverse this rejection.

Claim 1 recites:

> 1. A method comprising:
> detecting an update to a register file accessible by a plurality of processing elements of a media signal processor when a processing element desires ownership of a selected hardware accelerator;
> enabling the hardware accelerator selected from a plurality of hardware accelerators in response to at least one bit of a register within the register file that is set by the processing element to request ownership of the selected hardware accelerator; and
> granting the processing element ownership over the selected hardware accelerator. (Emphasis added.)

Dao is generally directed to a system for multimedia processing, where a data traffic master provides shared memory connections to one or more processing units. (See Abstract.) FIG. 2 of Dao describes an architecture that includes three portions, a memory portion 202, a

data portion (traffic master) 204, and a processor portion 206. (See col. 3, lines 38-40.) The traffic master of Dao coordinates all inter-processor, inter-memory, and processor-memory communications subject to programmed privileges to the page-based shared memory 322. (See col. 4, lines 4-8 and col. 5, lines 22-28.) Dao further indicates that processor units assert an enable signal to send or receive data. When the traffic master is ready to transfer or receive data, the traffic master asserts a ready signal. (See col. 4, lines 44-56.)

In contrast with Claim 1, Dao does not disclose detecting an update to a register file accessible by a plurality of processing elements of a media signal processor when a processing element desires ownership of a selected hardware accelerator. Dao describes a memory management unit (MMU) which processes addresses in conjunction with page pointers to determine the memory module accesses being attempted by processors. (See col. 5, lines 65-67.) As described by Dao, MMU registers are part of a logically mapped memory space that is used by the processors to perform mailbox message communication between the processors.

Dao does describe a mailbox message communication between processors (see col. 6, lines 57-60), however, that is something different from detecting an update to a register file accessible by a plurality of processing elements of a media signal processor when a processing element desires ownership of a selected hardware accelerator, as in Claim 1. Moreover, the MMU registers of Dao track such things as read/write execution permissions of each processor. Dao indicates that when a processor attempts to write to an MMU without write permission, an ICU 412 can assert and interrupt to alert one of the processors of the memory protection violation. (See col. 6, lines 37-40 and 64-65.) However, assertion of the interrupt is different from detecting a register file update when a processing element desires ownership of a selected hardware accelerator, as in Claim 1.

Furthermore, Dao does not disclose or suggest enabling a hardware accelerator in response to at least one bit of a register within a register file that is set by a processing element to request ownership of the selected hardware accelerator, as in Claim 1. According to the Examiner, Dao discloses that when a processor unit (e.g., a DSP) desires to access another processor unit (such as hardware accelerator) through the traffic master 204, the request processor unit should provide (besides address and data) an enable signal. (See col. 4, lines 32-

53.) (See page 3, para. 2 of the Office Action mailed 1/22/08.) The passages indicated by the Examiner refer to the sending or receiving of data by the array of processors 206 to and from the various memory shown, for example, as part of shared memory 202/322, as shown in FIGS. 2 and 3. However, the sending/receiving of data by the array of processors 206 to/from shared memory 322 is different from enabling of a selected hardware acceleration in response to a bit of a register file that is set by a processing element to request ownership of a selected hardware accelerator, as in Claim 1.

We submit that the assertion of an enable signal to send/receive data does not disclose, teach, or suggest enabling a selected hardware accelerator from a plurality of hardware accelerators in response to at least one bit of a register within a register file that is set by a processing element to request ownership of the selected hardware accelerator, as in Claim 1. Furthermore, the assertion of a ready signal by traffic master 204 for handling the sending/receiving of data between processors 206 and shared memory 322 does not disclose granting the processing element ownership over the selected hardware accelerator, as in Claim 1.

For each of the above reasons, Claim 1, and all claims which depend from Claim 1, are patentable over the cited reference Dao as well as the references of record.

Each of Applicants' other independent claims includes limitations similar to those in Claim 1 discussed above. Therefore, all of Applicants' other independent claims, and all claims which depend on them, are also patentable over the cited art, for similar reasons. Consequently, we request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 1, 3-6, and 8-26.

III. Claim Rejections Under 35 U.S.C. §103

Claim 27 is rejected under 35 U.S.C. §10103(a) as being unpatentable over Dao in view of U.S. Patent Publication No. 2003/0028751 to McDonald et al. ("McDonald"). Applicants respectfully traverse this rejection.

DEPENDENT CLAIMS

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as an agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 4/22/08

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CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____ 4/22/08
Elaine Kwak Date